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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,291	03/03/2004	Shadi A. AbuGhazaleh	44390	3538

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ROYLANCE, ABRAMS, BERDO & GOODMAN, L.L.P.
1300 19TH STREET, N.W.
SUITE 600
WASHINGTON,, DC 20036

EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,291	ABUGHAZALEH ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-23* is/are rejected.

7)☒ Claim(s) *9,10,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1104//01 Nov 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

2. Claims 1-8 and 11-23 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of Claims 1-3, 7-11 and 13-25 of copending Application No. 11/038,460. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Allowable Subject Matter

3. Claims 1-25 contain allowable subject matter.

4. Claims 9, 10, 24 and 25 are objected to because Claims 9 and 10 depend from rejected base Claim 1, and Claims 24 and 25 depend from rejected base Claim 15. Claims 9, 10, 24 and 25 MAY be allowable, the patentability of these dependent claims at least partly resting on how the Applicant amends the claims of the instant Application and the claims of copending Application 11/038,460, in view of the provisional statutory double patenting rejection under 35 U.S.C. § 101 set forth in this Office action and in the Office Action of the copending Application 11/038,460.

5. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 1-14, patentability resides in *at least one of a removable modular or fixed electronic component, said component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of the multilayered patch panel printed circuit board*, in combination with the other limitations of base Claim 1.

As to Claims 15-25, patentability resides in *disposing upon at least a second layer of the plurality of layers of the multilayered patch panel printed circuit board at least one of a removable modular and fixed electronic component, said component comprised of at least one active circuit*, in combination with the other limitations of base Claim 15.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Phommachanh (US 6,089,923) discloses all the limitations of originally filed base Claims 1 and 15 (multilayer patch panel 40 in Fig. 5; layers 1-4 in Figs. 6-9, respectively, a communication circuit on each layer containing signal carrying traces and compensation circuitry that includes conductive lines 52 disposed in parallel to form capacitors 52C; RJ45 connectors connected to one side of board 40 and IDC connectors mounted on the opposite side, the RJ45 connectors and IDC connectors interconnected through the compensation circuitry; col.4: 50-63; col.5: 58-col.7: 17;

Category 6 crosstalk suppression standards are met: col.2: 17-30 and col.8: 23-29) with the exception of *at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 40.*

b) Aekins (US 5,931,703) discloses all the limitations of originally filed base Claims 1 and 15 (including a three layer patch panel circuit board 20 in Fig. 2 labeled as layers 66, 67 and 68--see Figs. 3-5; col.4: 26-31; col.5: 54-59--wherein a communication circuit, containing signal carrying traces and compensation circuitry, is disposed on at least a first layer of board 20--see col.5: 26-48--and wherein middle layer 67 is a compensation separation mechanism disposed between the first and second layers 66 and 68: see col.6: 14-28; Category 5 crosstalk suppression standards are met: col.3: 48-58) with the exception of *at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 40.*

c) Aekins (US 6,057,743) discloses all the limitations of originally filed base Claims 1 and 15 including RJ45 and IDC connectors mounted on a multilayer patch panel circuit board 20 (Fig. 1; col.2: 40-46; col.4: 3-7) and a communication circuit, containing signal carrying traces and compensation circuitry on at least a first layer of the plurality of layers in patch panel board 20 (Figs. 2-5; col.5: 27-49), the compensation circuitry including capacitive and inductive structures formed from the conductive traces of the circuitry (col.5: 55-64; col.6: 16-29); Category 4, 5, 5e and 6 crosstalk suppression standards are met (col.2: 47-53; col.6: 48-col.7: 11). Aekins does not teach

at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 20.

d) Bullivant et al. (US 5,944,535) discloses all the limitations of originally filed base Claims 1 and 15 including the compensation layer 67 on a patch panel circuit board 28 having three circuit layers 66, 67 and 68, similar to the structure of Aekins (US 6,057,743), discussed above, and meeting Category 5 crosstalk suppression standards (col.5: 39-45).

e) Aekins (US 6,533,618 B1) discloses all the limitations of originally filed base Claims 1 and 15 (including the RJ45 and IDC connectors mounted on patch panel circuit board 4 (Fig. 3; col.6: 39-42) and a communication circuit containing signal carrying traces and compensation circuitry on the top and bottom surfaces of the patch panel board 4 (Figs. 4 and 5; col.7: 36-45; col.8: 13-64) but does not teach *a compensating separation mechanism comprised of a third layer disposed between the first (top) and second (bottom) layers of patch panel board 4* and does not teach *at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 4.*

f) Chen (US 6,483,715 B1) discloses all the limitations of originally filed base Claims 1 and 15 (RJ45 and IDC connectors and a patch panel circuit board 20 with a communication circuit disposed on both sides of board 20 containing signal carrying traces and compensation circuitry on the two sides of the circuit board 20, the

compensation circuitry formed as part of the interconnection circuitry and including capacitors 41, 42 and inductors 51a,b 52a,b formed integrally with the conductive lines of the interconnection circuitry; Figs. 2A,B and 3A,B; col.2: 66-col.3: 2; col.3: 53-col.4: 63; category 6 crosstalk suppression standards are met: col.2: 11-13) with the exception of *a compensation separation mechanism comprised of at least a third layer disposed between the first and second layers* and *at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 20.*

g) Hipp et al. (US 6,411,506 B1) discloses a passive midplane 34 with DIMMs (col.9: 27-34; col.10: 28-38) and CPUs (col.7: 63-col.8: 5) connected to one side and network interface cards connected to the opposite side (Figs. 1 and 4-7; col.3: 44-col.4: 27) using RJ45 connectors (col.12: 13-19); Category 5 communication cable 44 is used (col.12: 9-13); industry standard rack of 42 U is employed (col.8: 57-64); passive midplane 34 auto-senses CPU cards and available connector slots to allow automatic configuration of networks via remote management system 70 (col. 15: 43-50).

h) Berding (US 5,930,119) discloses a passive backplane having compensation circuitry that reduces LC product inherent in the conductive traces, thereby reducing signal propagation delay (Figs. 2-5; col.5: 31-61; col.6: 33-39).

i) Berding (US 6,512,396) discloses a backplane with compensation circuitry (Fig. 5) and active components--i.e., boost circuits 200 and 204 (Figs. 5 and 6)--for reducing signal rise and fall times (col.4: 55-col.5: 28) and passive components--i.e., damping

resistors 903 (Fig. 5)--for line termination and elimination of signal reflection (col.6: 18-50).

j) Balakrishnan (US 4,697,858) discloses an active backplane having removable daughterboards 108 on one side and transceiver chips 106 on the opposite side, the placement of the transceivers 106 on the backplane saving space on the daughterboards and improving the electrical performance of the backplane (col.6: 37-41); the backplane including ground planes 112 and 114 for shielding bus lines 110 and reducing crosstalk (col.4: 28-33; col.5: 45-51).

k) Thompson et al. (US 5,748,451) discloses, in Figs. 1 and 3, an active backplane 12 (col.1: 11-25) provided with a stiffener (substrates 14 and 16), the stiffener substrate 16 having connectors 22--for receiving removable voltage regulator cards or power supply cables in order to provide power or other signals to active backplane 12--and further having decoupling capacitors 26 mounted thereon for power and/or signal line noise suppression (col.3: 10-30). Active backplane 12 has cards 32 mounted directly thereto (Fig. 3; col.3: 65-col.4: 29).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
July 20, 2005